ADVANCED VLSI DESIGN AND TECHNOLOGY

UNIT –I

Introduction to MOS technology: Introduction to IC technology, MOS and related VLSI technology, NMOS, CMOS, BiCMOS Technologies, Thermal aspects of processing, Production of E beam marks.

UNIT –II

Circuit design processes and Scaling of MOS Circuits: MOS layers, Stick diagrams, Design rules, and layout, 2 & 1.2 micro meter CMOS rules, Layout diagrams, Symbolic diagram,Scaling models, Scaling function for device parameters, Limitations of scaling.

UNIT –III

Basic Circuit concepts and sub system design: Sheet resistance, Area capacitances of layers, Delay unit, Wiring Capacitances, Choice of layers.

Architectural issues, Switch logic, Examples of Structural design (Combinational logic).

UNIT –IV

Sub system design process: Design of ALU subsystem, Some commonly used storage elements, Aspects of design tools, Design for testability, Practical design for test guidelines, Built in self test, CMOS project-an incrementer / decrementer, a comparator for two n-bit numbers. Ultra fast systems, Technology development, MOSFET based design.

UNIT –V

The mos inverter, layout and simulation:Inverter principle, Depletion andenhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption. MOS SPICE Model, Device Characterization, Circuit Characterization, Interconnects and Simulation. MOS Device Layout, Transistor Layout, Inverter Layout, CMOS Digital Circuits Layout & Simulation

TEXT BOOKS: 1.Basic VLSI Design by Douglas A, Pucknell, Kamran Eshraghian, PrenticeHall, l996, 3rd Edition.

2. Kang &Leblebigi “CMOS Digital IC Circuit Analysis & Design”- McGraw Hill, 2003

References:

1. Mead, C.A and Conway, LA, “Introduction to VLSI Systems”, AddisonWesley, Reading, Massachusetts, l980.

MODEL QUESTION PAPER

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Answer any five questions.All questions carry equal marks

1. a) With neat sketch explain BICMOS fabrication in an n-well process. [8]

b) Draw the symbolic layout for the CMOS inverter and write the general CMOS logic gate layout guidelines. [8]

2. a) What is stick diagram and explain about different symbols used for components in Stick diagram. Draw the stick and layout for a two input CMOS NAND gate. [8]

b) Explain different forms of pull-ups used as load in CMOS enhancement. [8]

3. a) Determine pull-up to pull-down ratio of an NMOS inverter when driven through one or more pass transistors. [8]

b) Write about the scaling limitations due to sub threshold currents in MOSFETS. [8]

4. a) Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [8]

b) What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors. [8]

5. a) Explain the architectural issues of subsystem design. [8]

b) Explain the structural design approach with an example. [8]

6. a) What is the need of testability? Explain design for testability. [8]

b) Describe the decoder based selection and control RAM arrays with a neat diagram. [8]

7. a) Explain MOSFET SPICE models indetail. [8]

b) What is latch-up condition in CMOS circuits? How it can be eliminated[8]

8.Write short notes of the following: [16]

a) Power consumption
b) Noise margin
c) Propagation delay and
d) Dynamic behavior of CMOS inverter